(12) UK Patent Application (19) GB (11) 2 269 049 (13) A

(43) Date of A Publication 26.01.1994

(21) Application No 9304655.5

(22) Date of Filing 08.03.1993

(30) Priority Data
(31) 9212438 (32) 13.07.1992 (33) KR

(51) INT CL[5]
H01L 27/108 // G11C 11/409

(52) UK CL (Edition M)
H1K KGAFX K1CA K1FL K11A3 K11B3 K11C1A K11D K4C11 K4C14 K4C2B K9D1 K9R2
G4C C11409
U1S S2121

(56) Documents Cited
WO 90/08401 A US 5157281 A
JAPIO ABSTRACT OF JP62-155555, & JP62-155555 (SONY)

(58) Field of Search
UK CL (Edition L) H1K KGAF KGAM
INT CL[5] H01L

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(54) Semiconductor memory device

(57) An integrated semiconductor RAM memory cell array region (100) and peripheral circuit region (400) incorporates a triple well structure comprising a first n-type well (22, 81) formed in a p-type substrate (70) and biased by a first bias voltage (Vcc), a p-type well (23, 83) formed in the first well and biased by a second bias voltage (Vbb), and a further n-type well, which is a region of an MOS transistor, formed in the p-type well and connected to the second bias voltage. The substrate may be arranged to receive a third bias voltage.

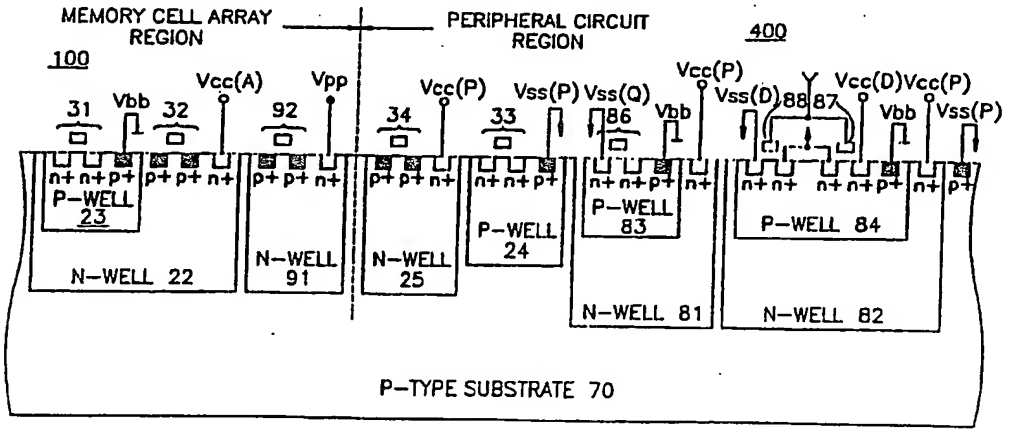
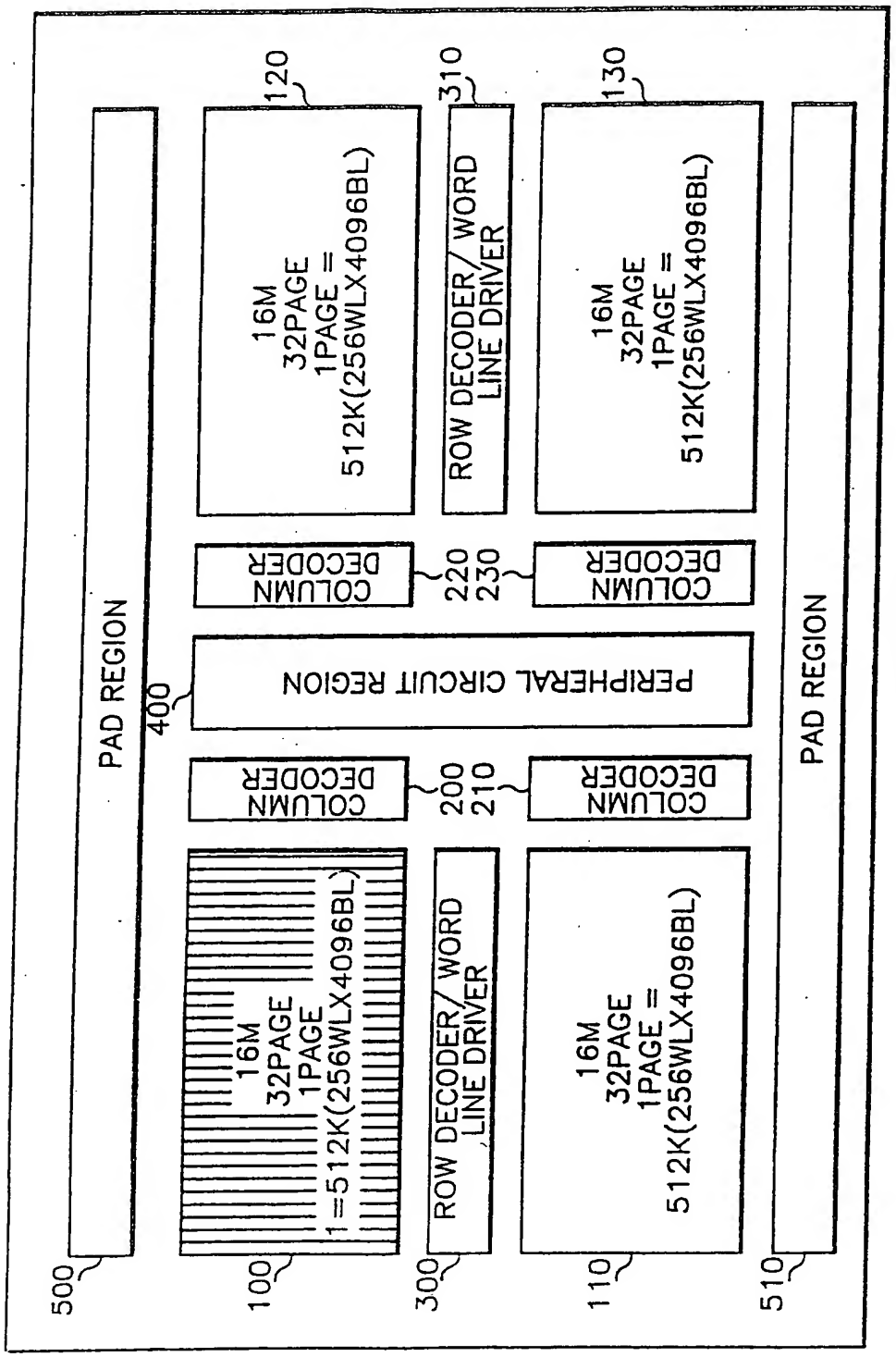


FIG. 6

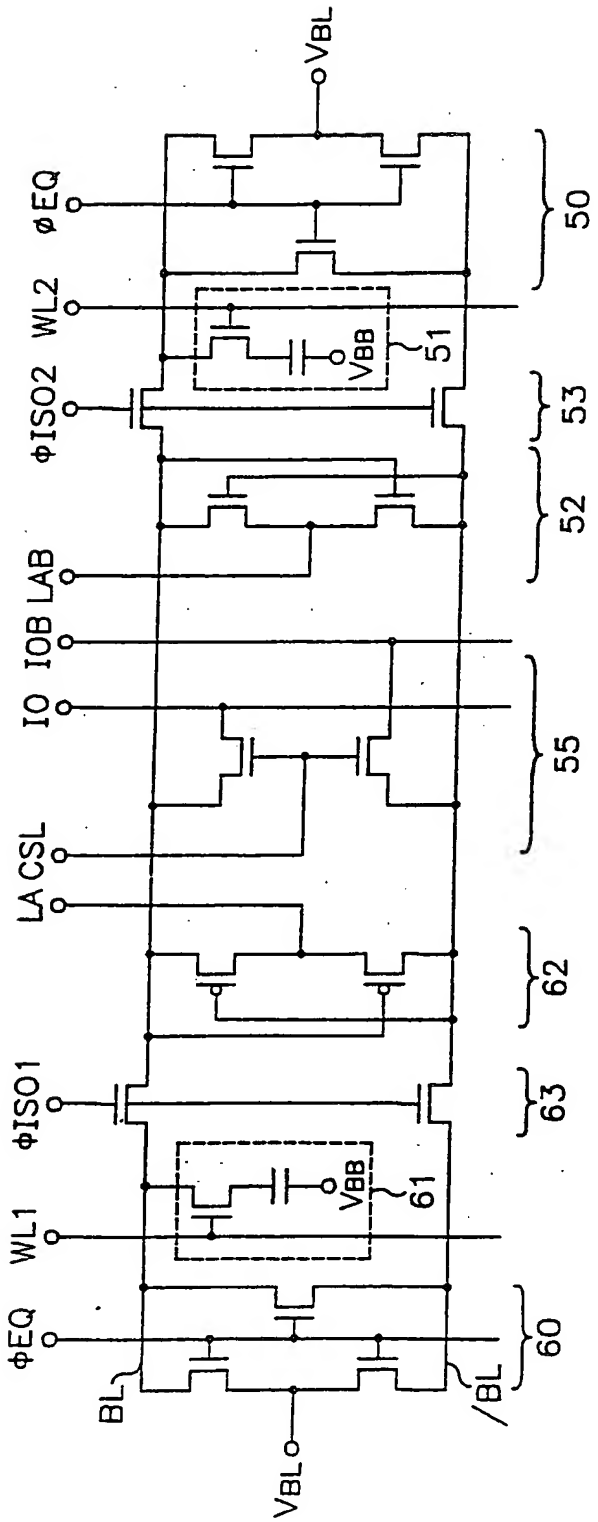
GB 2 269 049 A

DG

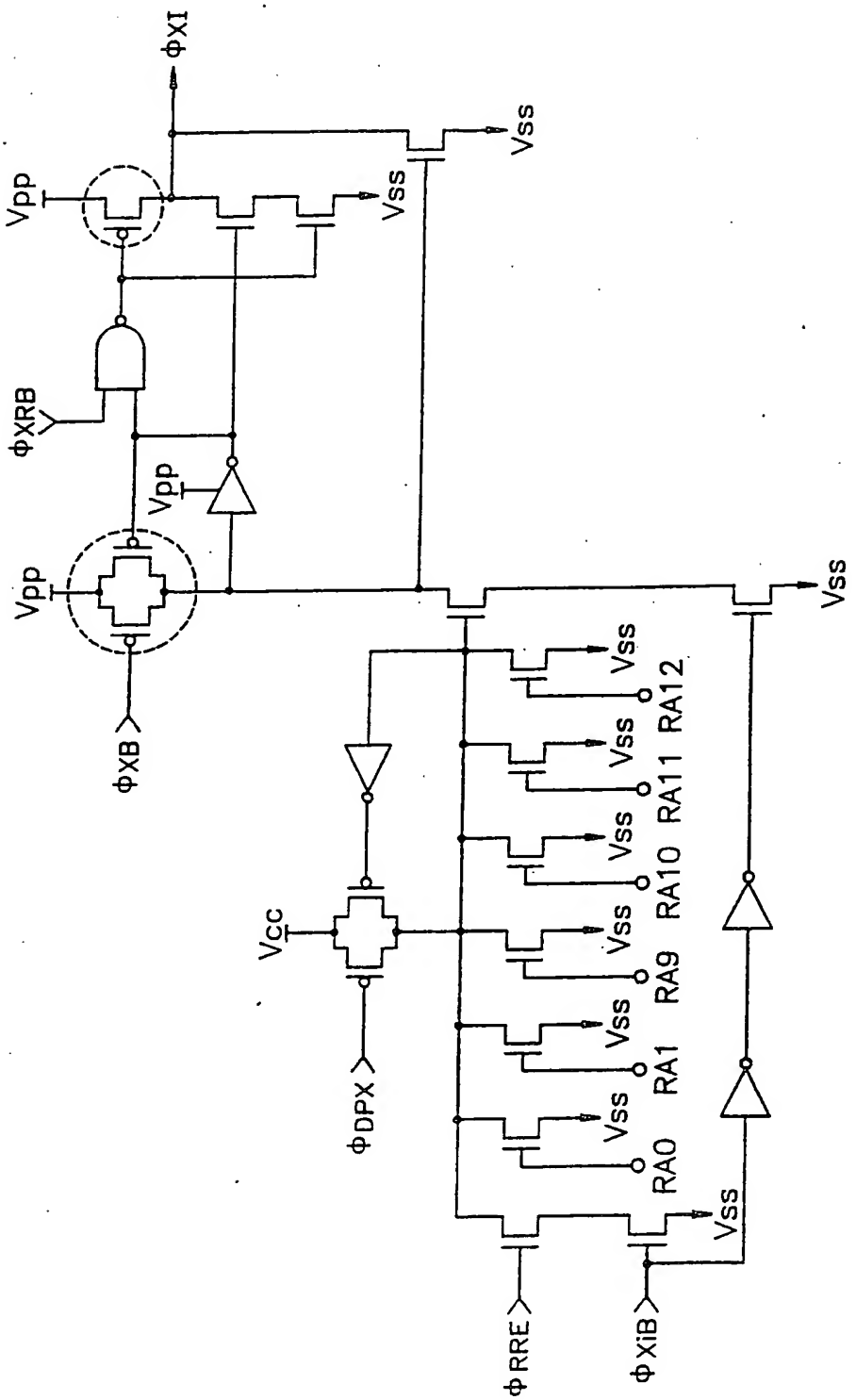


(PRIOR ART)

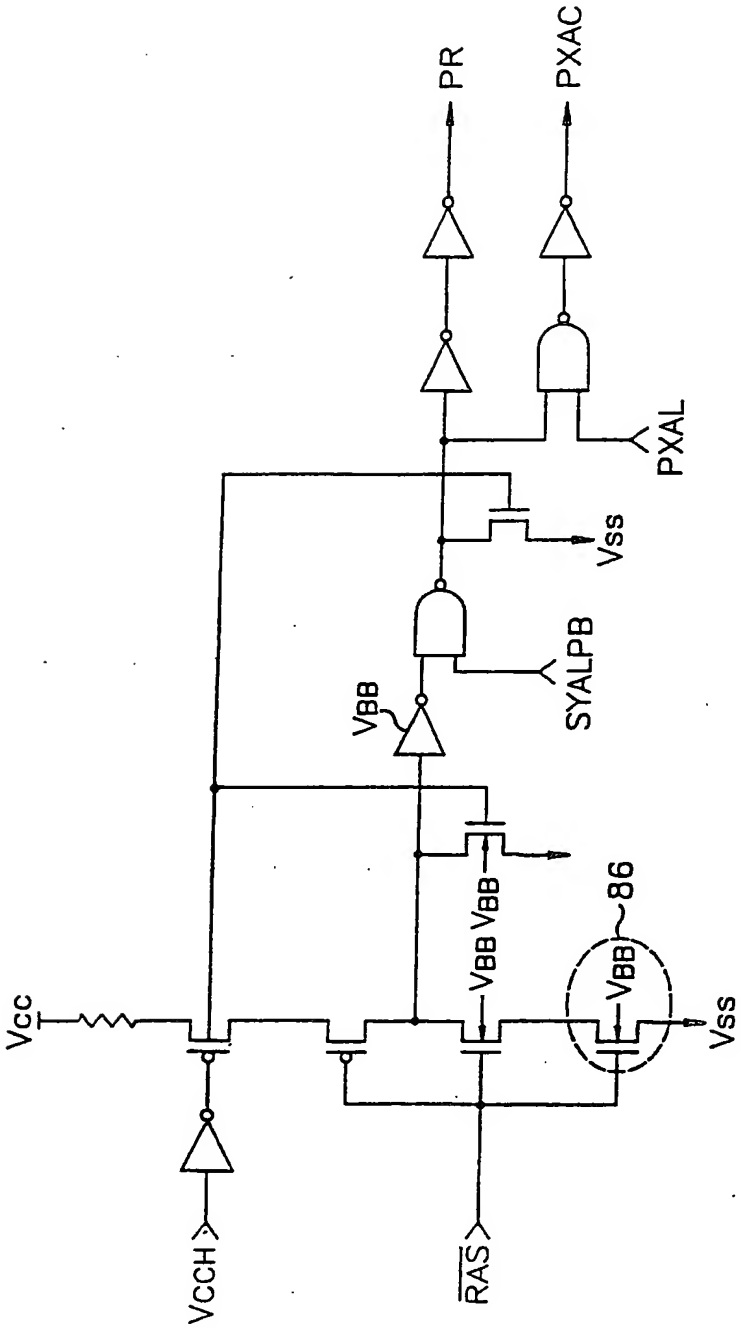
FIG. 1A



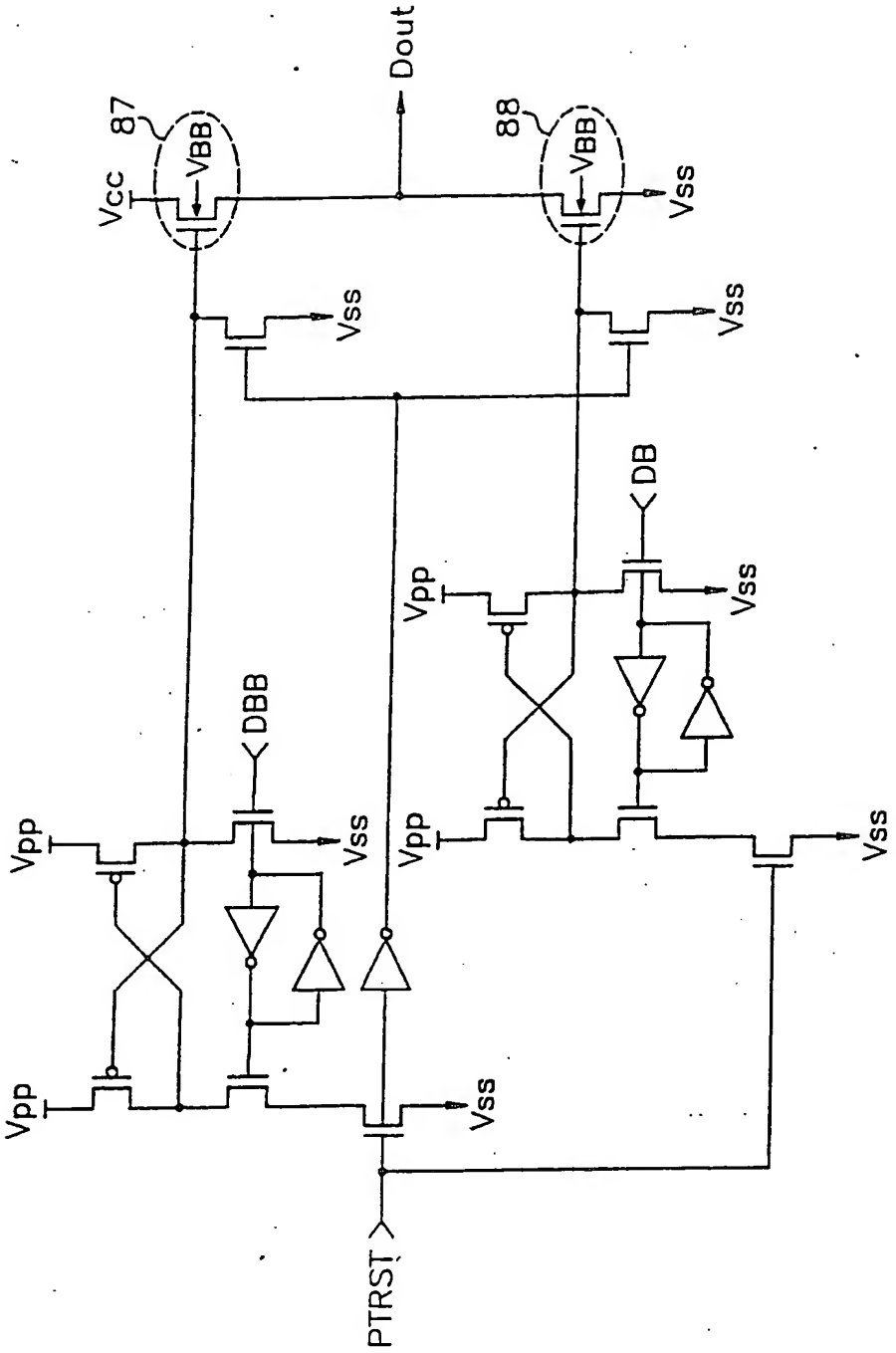
(PRIOR ART)
FIG. 1B



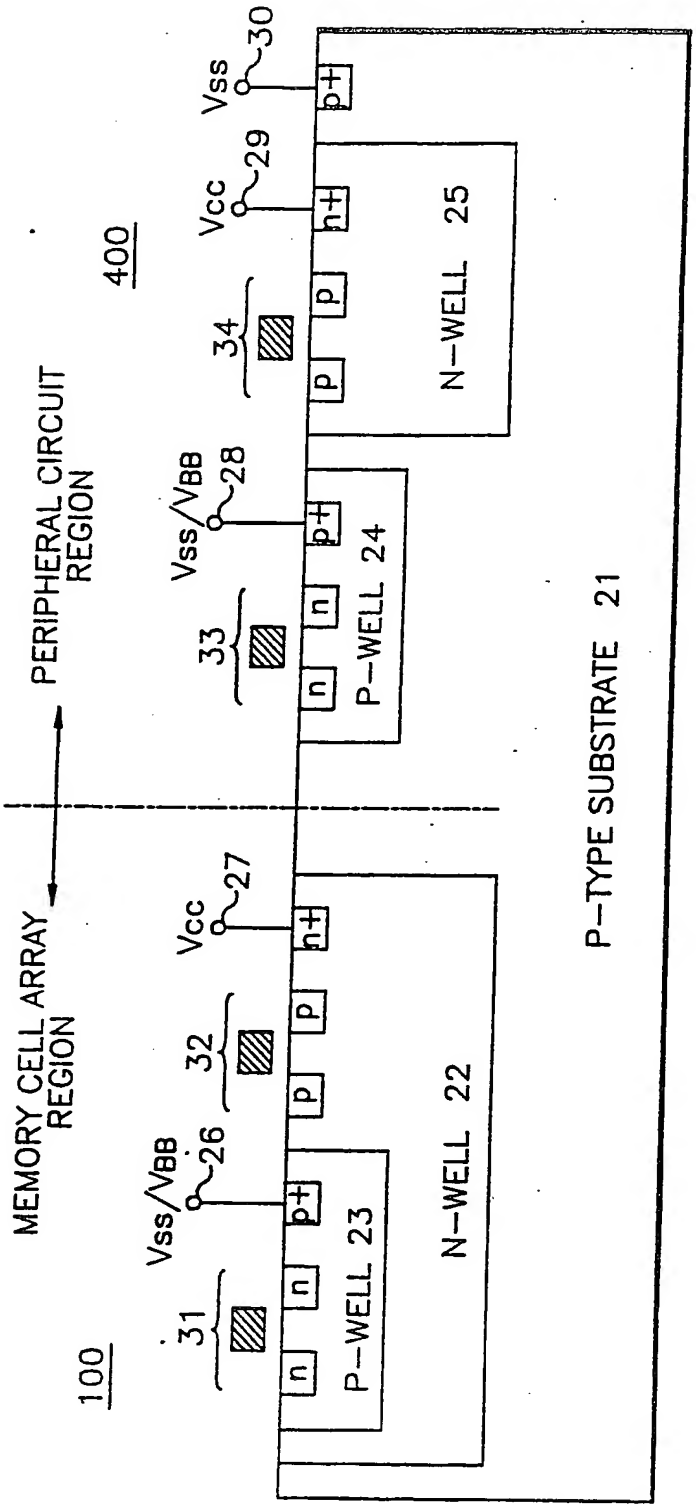
(PRIOR ART)
FIG. 1C



(PRIOR ART)
FIG. 1D



(PRIOR ART)
FIG. 1E



(PRIOR ART)
FIG. 2

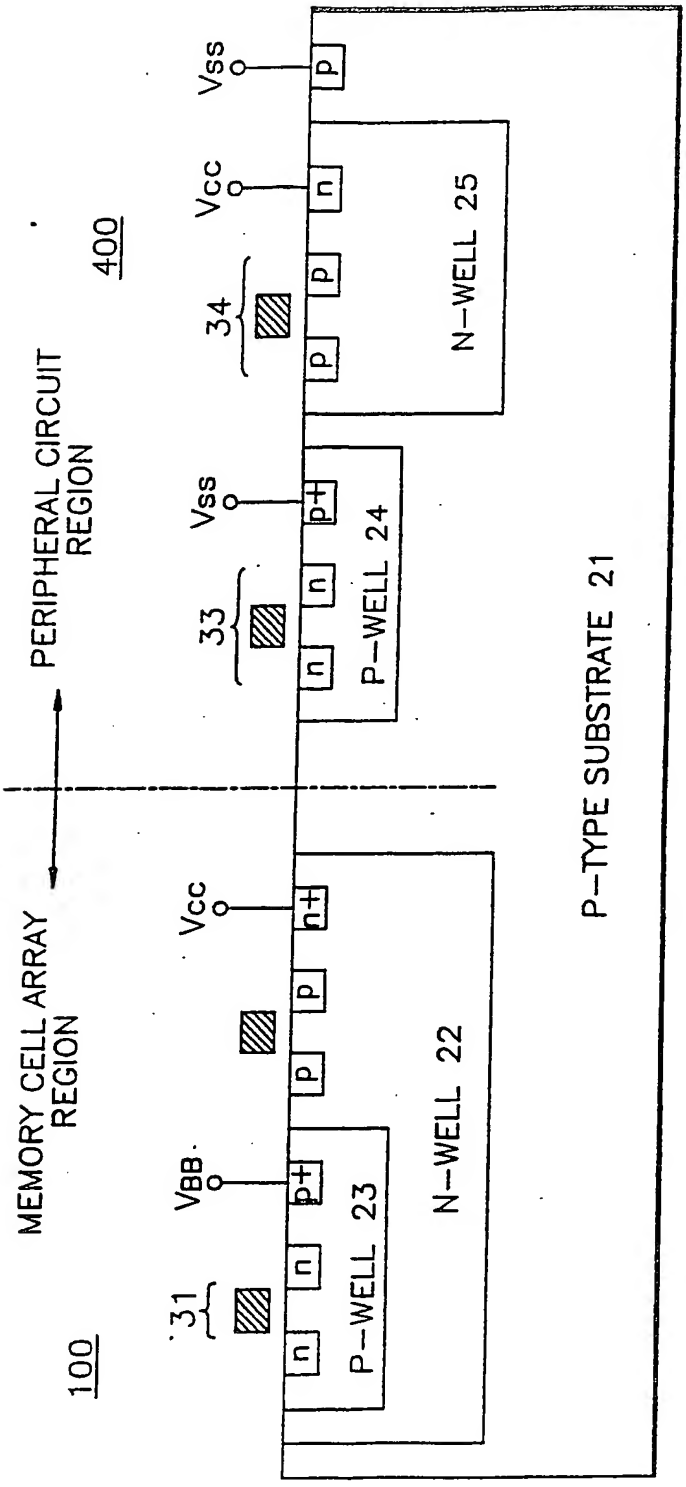

100
MEMORY CELL ARRAY REGION
400
PERIPHERAL CIRCUIT REGION
31
33
34
VBB
Vcc
Vss
n+
p+
n
p
P-WELL 23
N-WELL 22
P-WELL 24
N-WELL 25
P-TYPE SUBSTRATE 21

FIG. 3A

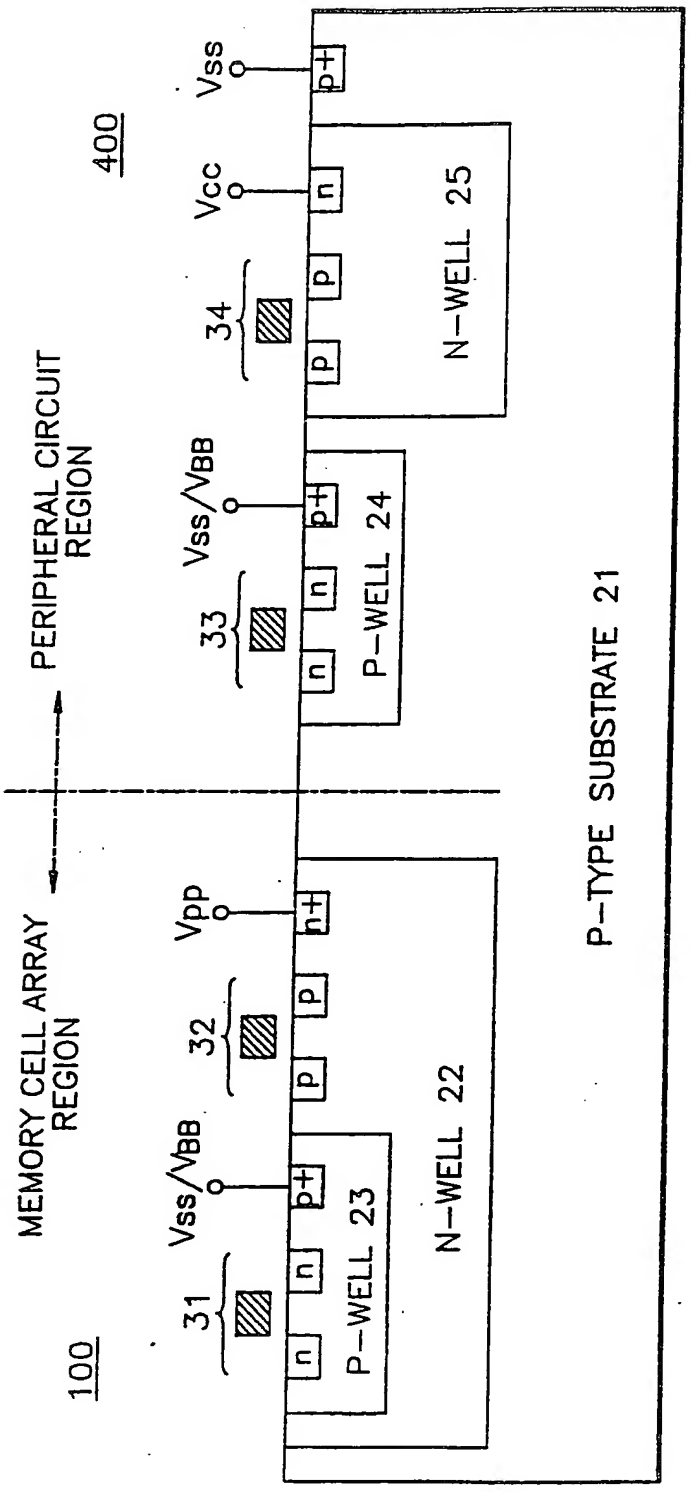

100
400
MEMORY CELL ARRAY REGION
PERIPHERAL CIRCUIT REGION
P-TYPE SUBSTRATE 21
N-WELL 22
P-WELL 23
N-WELL 25
P-WELL 24
Vss/VBB
Vpp
Vcc
Vss
31
32
33
34
n+
p+
n
p

FIG. 3B

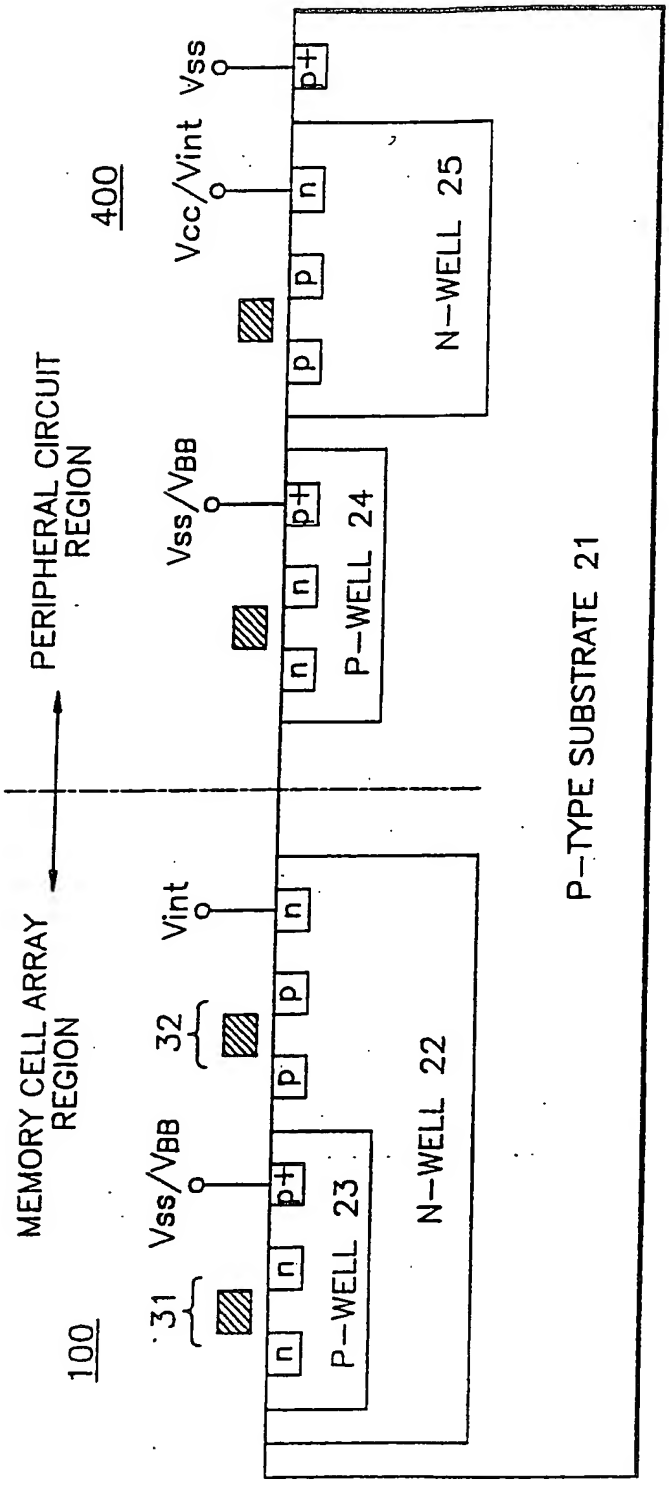

100
400
MEMORY CELL ARRAY REGION
PERIPHERAL CIRCUIT REGION
31
32
Vss/VBB
Vint
Vcc/Vint
Vss
n
p
p+
P-WELL 23
P-WELL 24
N-WELL 22
N-WELL 25
P-TYPE SUBSTRATE 21

FIG. 3C

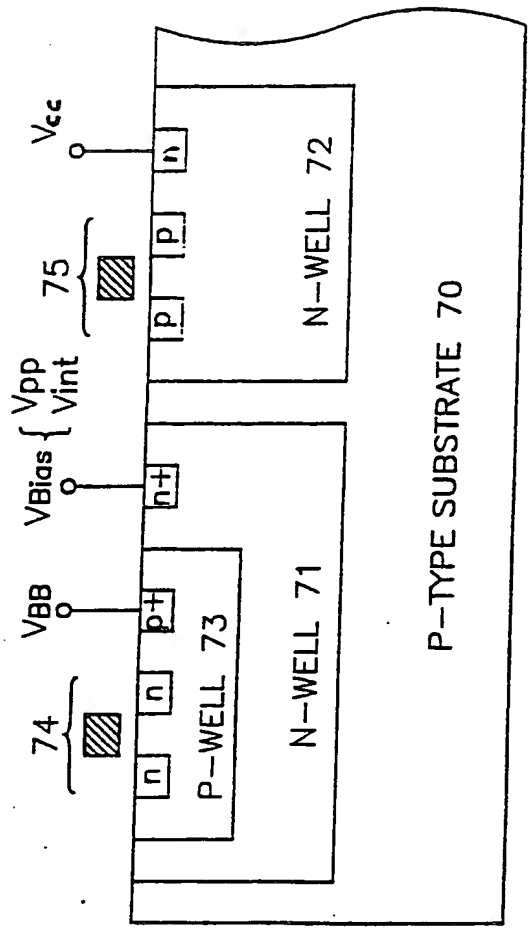

Vcc
75
Vpp
Vint
VBias
VBB
74
n
p
n+
p+
P-WELL 73
N-WELL 71
N-WELL 72
P-TYPE SUBSTRATE 70

FIG. 4A

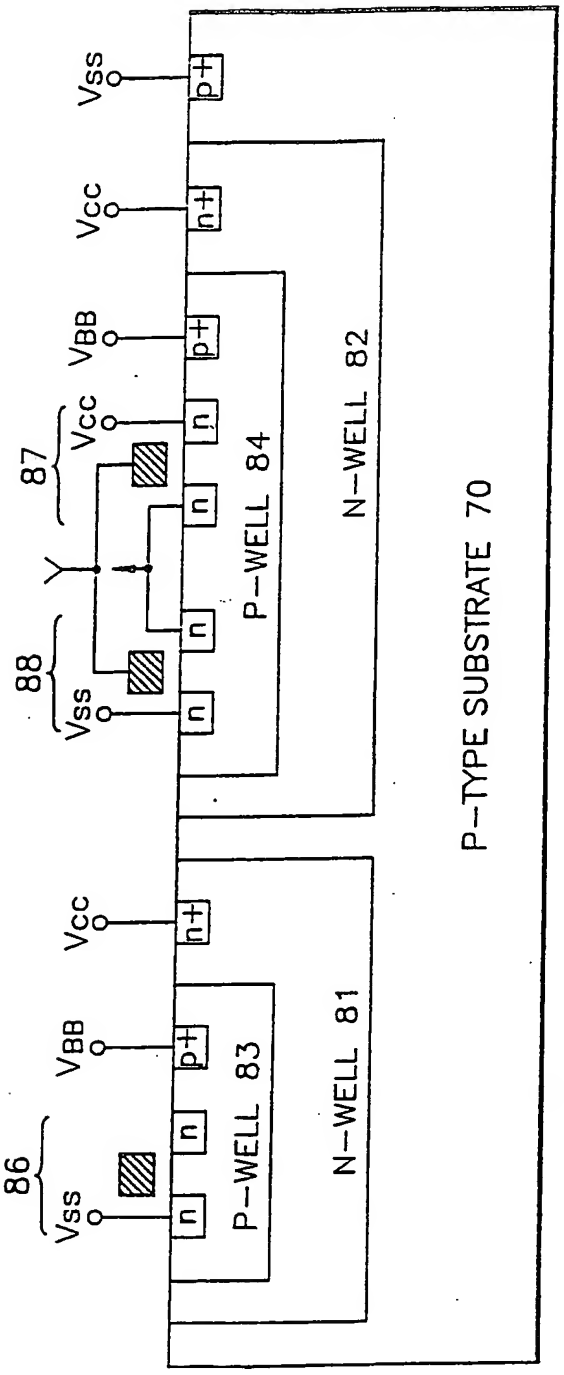

Vss
Vcc
VBB
Vcc
87
Y
88
Vss
Vcc
VBB
86
Vss
p+
n+
p+
n
n
n
n
p+
n+
n
P-WELL 84
N-WELL 82
P-TYPE SUBSTRATE 70
N-WELL 81
P-WELL 83

FIG. 4B

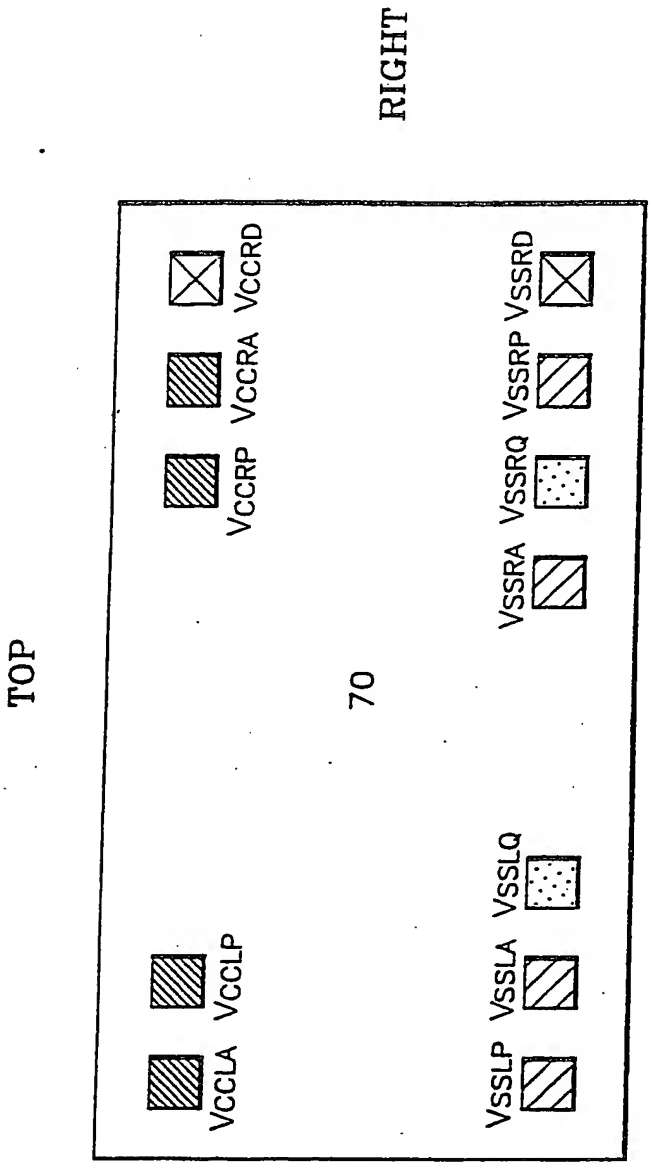

TOP
RIGHT
LEFT
BOTTOM
70
VCCLA
VCCLP
VCCRP
VCCRA
VCCRD
VSSLP
VSSLA
VSSLQ
VSSRA
VSSRQ
VSSRP
VSSRD

FIG. 5

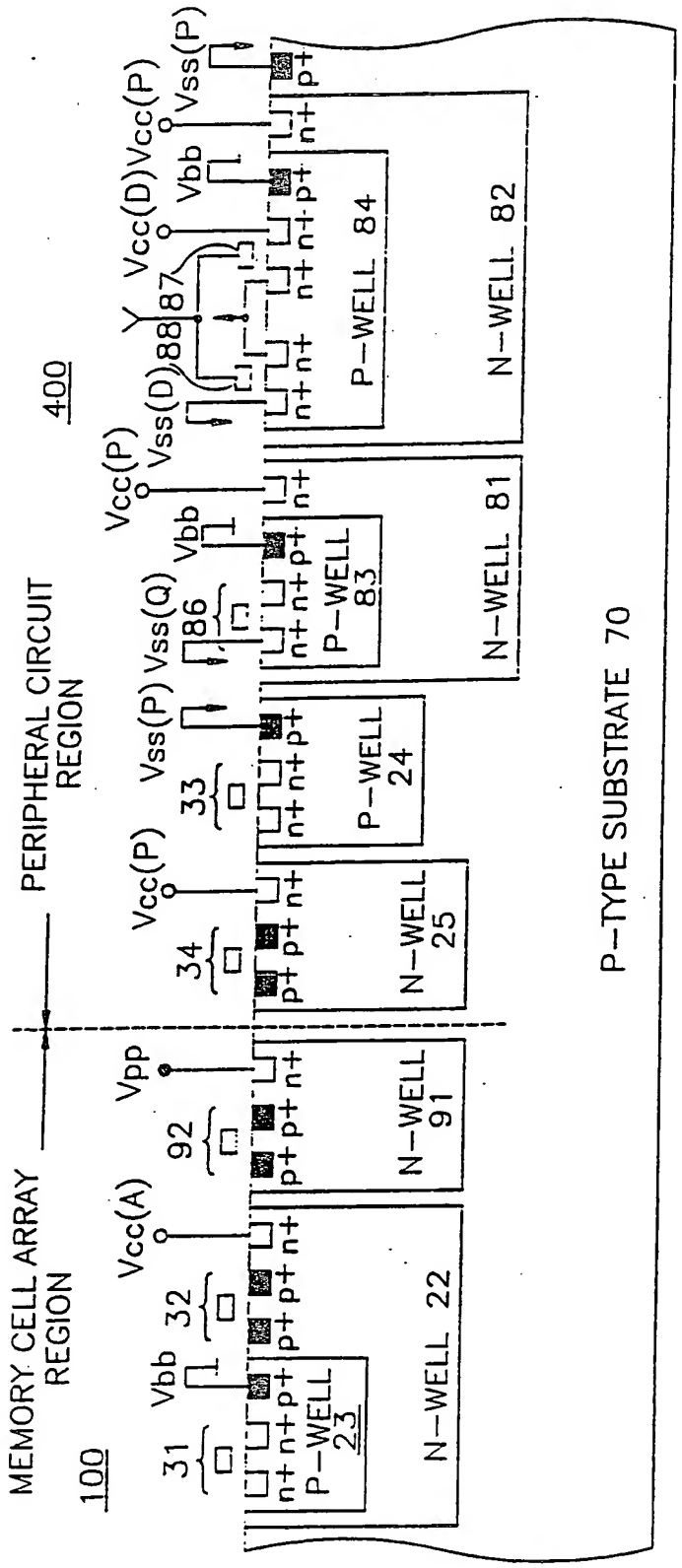

MEMORY CELL ARRAY REGION
100
PERIPHERAL CIRCUIT REGION
400
P-TYPE SUBSTRATE 70
N-WELL 22
P-WELL 23
N-WELL 91
N-WELL 25
P-WELL 24
N-WELL 81
P-WELL 83
N-WELL 82
P-WELL 84
Vcc(A)
Vpp
Vcc(P)
Vss(P)
Vss(Q)
Vbb
Vss(D)
Vcc(D)
31
32
33
34
86
87
88
92
n+ n+ p+
p+ p+ n+

FIG. 6

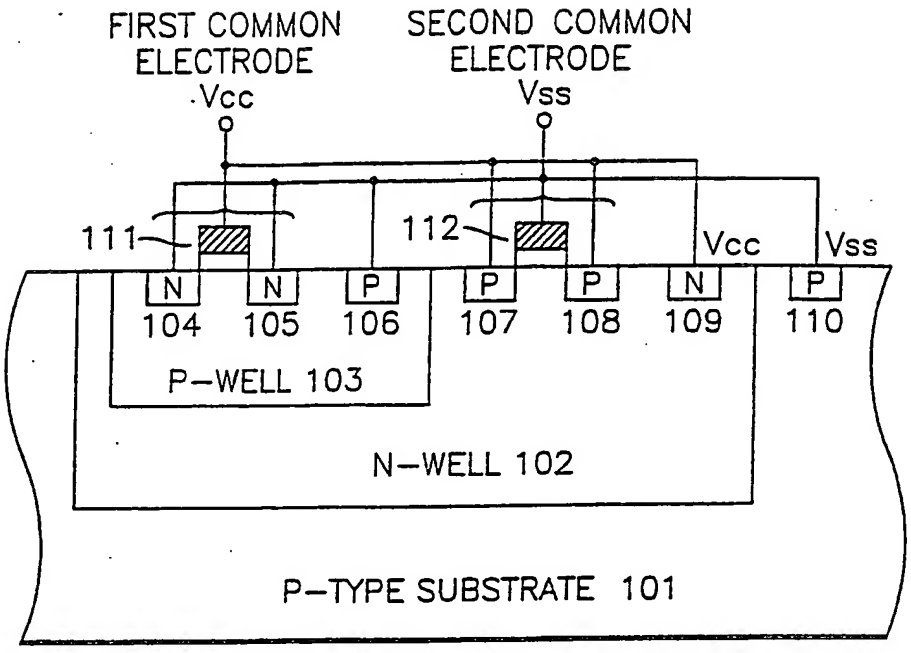

FIRST COMMON ELECTRODE
Vcc
SECOND COMMON ELECTRODE
Vss
111
112
Vcc
Vss
N
N
P
P
P
N
P
104
105
106
107
108
109
110
P–WELL 103
N–WELL 102
P–TYPE SUBSTRATE 101

FIG. 7A

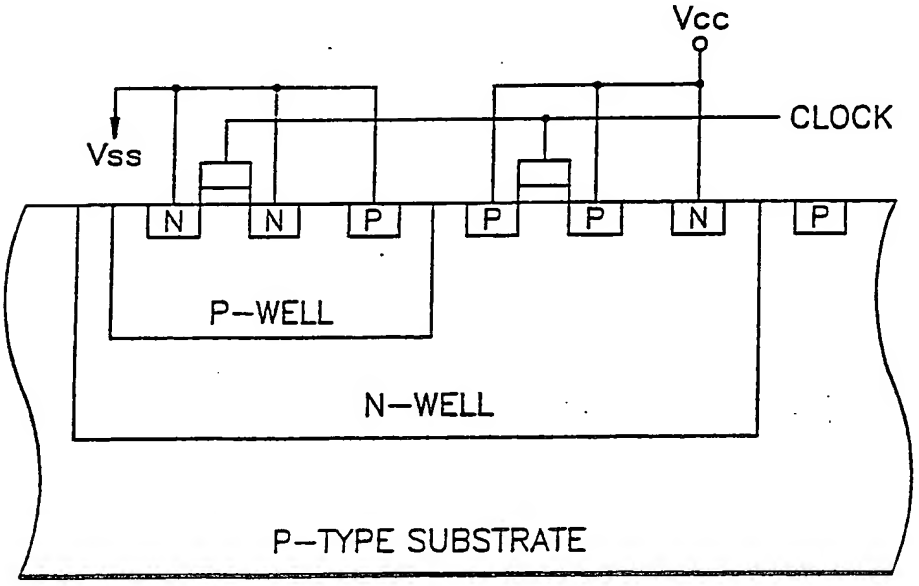

Vcc
CLOCK
Vss
N
N
P
P
P
N
P
P–WELL
N–WELL
P–TYPE SUBSTRATE

FIG. 7B

FIG. 8A

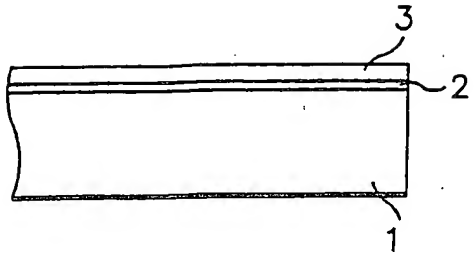


FIG. 8B

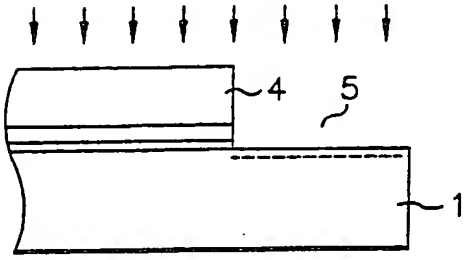


FIG. 8C

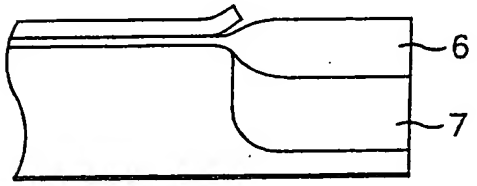


FIG. 8D

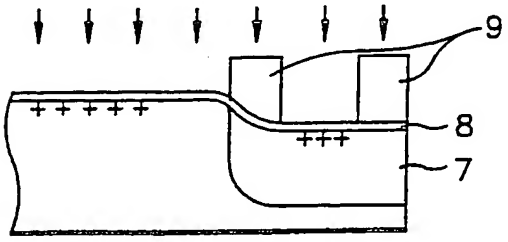
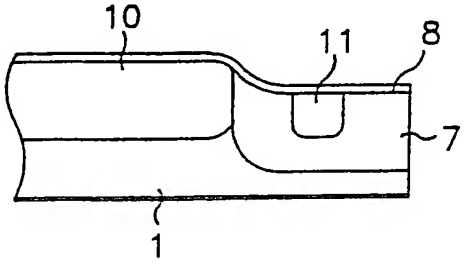


FIG. 8E



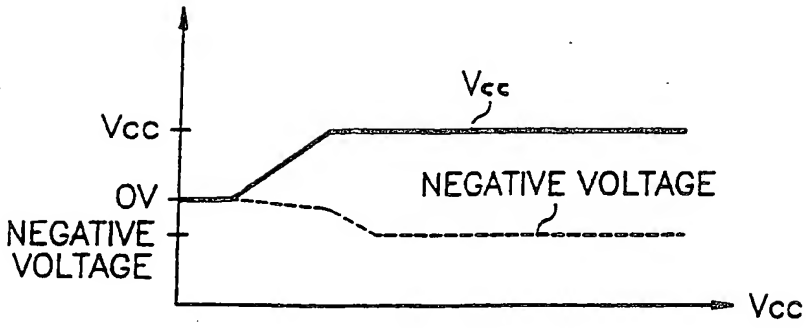


FIG. 9

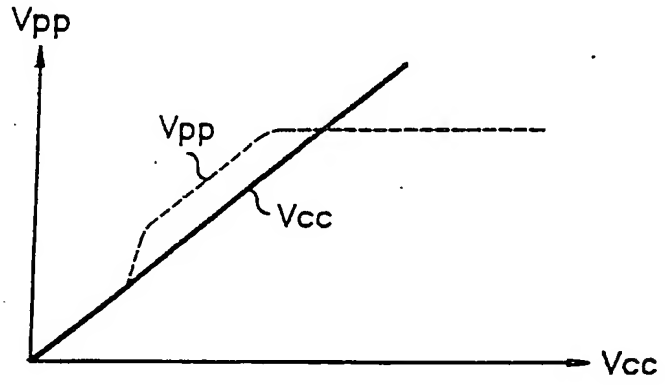


FIG. 10

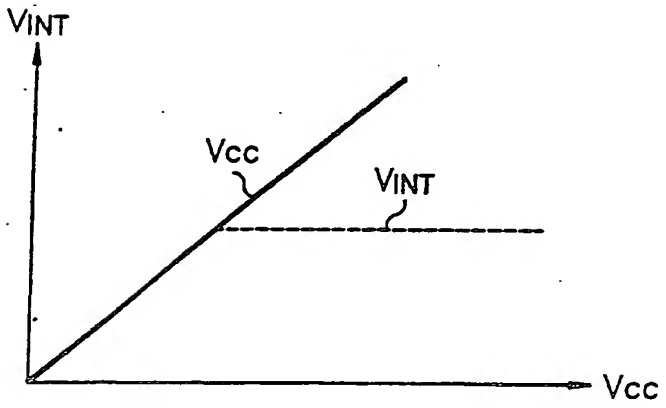


FIG. 11

SEMICONDUCTOR MEMORY DEVICE

The present invention relates to semiconductor devices, and more particularly to semiconductor memory devices with a triple-well structure.

As the capacity and density of semiconductor memory devices greatly increases, it becomes necessary to change the structure and process techniques of the devices. Practically, a three-dimensional structure has been employed in a semiconductor memory device with a capacity over 4 Mega bits so as to achieve a high complexity within a limited area. Additionally, as the size of MOS transistors used in semiconductor memory has been reduced, a lower internal source voltage has been employed. Further, noise problems are produced according to the high complexity. Of course, it is required that the memory device should operate with a minimum data access time for reduced power consumption.

A known Dynamic Random Access Memory (DRAM) device will now be described with reference to Figures 1 and 2 of the accompanying diagrammatic drawings, in which:

Figure 1A illustrates a structure of a DRAM of the order of 64 Mega bits, Figures 1B and 1C show bit line circuits and row decoder/word line drive clock pulse generator formed in a memory cell array region respectively, and Figures 1D and 1E show a TTL input buffer and data output buffer/driver formed in a peripheral circuit region respectively; and

Figure 2 is a schematic diagram for illustrating a conventional method of applying a well bias voltage to the memory cell array region and peripheral circuit region according to Figure 1.

Figure 1A shows a DRAM of the order of 64 Mega bits, which includes four memory cell array blocks of 16 Mega bits 100, 110, 120, 130, row decoder/word line driver blocks 300, 310, four column decoder blocks 200, 210, 220, 230 respectively connected with the four memory cell array blocks 100, 110, 120, 130, peripheral circuit region 400 and pad regions 500, 510. The memory cell array block 100 is provided with a plurality of memory cells, word lines, bit lines and sense amplifiers, while the peripheral circuit region 400 is provided with transistor- transistor-logic (TTL) input buffers, data output buffers and output drivers. The row decoder/word line driver regions 300, 310 are provided with a clock pulse generator for generating word line drive clock pulses. These are CMOS circuits consisting of a plurality of NMOS and PMOS transistors, which are formed by a plurality of wells and diffusion regions arranged on a single substrate or wafer. Figures 1B, 1C, 1D and 1E show typical circuits arranged in the memory cell array region 100 and peripheral circuit region 400 respectively. Figure 1B shows a circuit for bit lines, which includes bit line equalization circuits 50 and 60, memory cells 51 and 61, N-type and P-type sense amplifiers 52 and 62, separation gates 53 and 63, column gate 55, word lines WL1 and WL2, and bit lines BL and /BL. Likewise, a clock pulse generator of Figure 1C for generating clock pulses to drive a row decoder/word line includes a TTL input buffer of Figure 1D for $\overline{RAS}$, and a data output buffer/driver of Figure 1E, etc, are well-known in the art. However, it should be noted that the transistors 86. 87, 88 in the drawings applied with a backgate voltage V_{BB} are related to the present invention.

When fabricating a semiconductor memory device as shown in Figure 1A using a P-type substrate, an N-well with a PMOS transistor is formed in the substrate and an NMOS transistor is formed in the substrate. In this case, the substrate is applied with a substrate bias voltage of a given level, usually a ground voltage, and the N-well with a backgate voltage, sometimes referred to as "well bias voltage", to set the threshold voltage of the transistor. On the contrary, if the substrate is an N-type substrate with a P-type well, the P-type well is applied with the backgate voltage to adjust the threshold voltage of an NMOS transistor formed in the P-well. A technique related to the backgate voltage is, as disclosed in Korean Patent Application No. 86-6557, applied to a P-well with a cell transistor in order to prevent data leakage due to the differences between the threshold voltages of a word line drive transistor and the cell transistor. In fact, a memory device of high complexity at least over 16 Mega bits has millions of wells formed in the substrate, which wells are applied with a well bias voltage or backgate voltage whose value is set by the usage of the elements.

Figure 2 shows the application of a well bias voltage in a memory cell array region and peripheral circuit region. A triple-well structure consisting of N+/P/N shown in Figure 2 was disclosed in IEEE JSSC ("A 45ns 16Mbit DRAM with Triple-Well Structure, IEEE JSSC., Vol. 24, No. 5, Oct. 1989, pp.1170-1174). The memory cell array region 100 has an N-well 22 with a P-well 23. It is readily appreciated that an NMOS transistor 31 formed in the P-well 23 and a PMOS transistor 32 formed in the N-well 22 respectively constitute N-type and P-type sense amplifiers in the memory cell array region 100. Meanwhile, in the peripheral circuit region 400, an NMOS transistor 33 formed in a P-well 24 and a PMOS transistor 34 formed in an N-well 25 are respectively provided for a TTL input buffer and data output

driver. In the memory cell array region 100, a well bias electrode 26 of the P-well 23 (or a backgate electrode of the NMOS transistor 31) is applied with a ground voltage Vss or negative voltage V_{BB}, and a well bias electrode 27 of the N-well 22 (or a backgate electrode of the PMOS transistor 32) with a source voltage Vcc. In the peripheral circuit region 400, a well bias electrode 28 of the P-well 24 (or a backgate electrode of the NMOS transistor 33) is applied with the ground voltage Vss or the backgate voltage V_{BB}, and a well bias electrode 29 of the N-well 25 (or a backgate electrode of the PMOS transistor 34) with the source voltage Vcc. An electrode 30 of the P-type substrate 21 is grounded. The N-well 22 formed in the memory cell array region 100 electrically separates the P-well 23 and the P-type substrate 21 and prevents interference between the well bias voltages of the wells. This is an advantage of a triple-well employed in a memory device of high complexity.

However, if the well bias electrodes 26 and 28 of the P-wells 23 and 24 are applied with ground voltage Vss or backgate voltage V_{BB}, the following problems occur. First, with the ground voltage Vss, since most of the bit lines are formed on the P-well region in the memory cell array region, their electrostatic capacitance is increased so as to adversely increase the ratio C_B/Cs of bit line capacitance C_B to memory cell storage capacitance Cs. A bit line is connected with an N+ diffusion region that is a drain of the NMOS transistor 31 constituting a N-type sense amplifier of a current-mirror type formed in the P-well 23 of the memory array, as shown by the N-type sense amplifier 52 in Figure 1B. If the bit line capacitance is greater than the storage capacitance, the time for accessing the data of the memory cells is delayed. This is well-known in the art. Further, since the P-wells of the memory cell array region and peripheral circuit region are commonly applied with the ground voltage, the noise caused by the ground voltage in the

peripheral circuit region interferes with the ground voltage in the memory cell array region. This may adversely affect the operational characteristics of the memory cell array.

Second, if the well bias electrodes 26 and 28 are applied with the negative voltage V_{BB} and transistors with a short channel are used in the peripheral circuit region, the short-channel causes a drop of the threshold voltage before the negative voltage V_{BB} generated by a negative voltage generator reaches the desired normal voltage level, so that latch-up phenomenon may occur. The negative voltage is not maintained at a fixed level as the source and ground voltages, so that it requires a proper compensation for maintaining the normal voltage level by means of continuous feedback operation. An oscillator, charge pump, etc. are used to maintain the negative voltage at the desired normal voltage level. The latch-up phenomenon caused by the deviation of the negative voltage influences the parasitic elements formed by the parasitic junctions in the substrate, thus resulting in erroneous function of the semiconductor memory device.

Preferred embodiments of the present invention aim to provide a device for preventing erroneous function of a semiconductor memory device caused by voltage source noise between a memory cell array region and peripheral circuit region.

It is another aim to provide a device for providing stable electrical insulation between substrate and wells of a semiconductor device of high complexity.

According to one aspect of the present invention, there is provided a semiconductor device comprising:

a first second-conductivity-type well formed on a first-conductivity-type semiconductor substrate and arranged to receive a first bias voltage;

a first-conductivity-type well formed in said first second-conductivity-type well and arranged to receive a second bias voltage; and

a second second-conductivity-type well formed in said first-conductivity-type well and connected to said second bias voltage.

Preferably, said first-conductivity-type semiconductor substrate is arranged to receive a third bias voltage.

Preferably, said first-conductivity-type well may comprise an active region of a second-conductivity-type MOS transistor.

Preferably, at least one of said second-conductivity-type wells comprises a first-conductivity-type MOS transistor.

Another second-conductivity-type well may be provided with a first-conductivity-type MOS transistor isolated from said second-conductivity-type well and arranged to receive a fourth bias voltage.

Preferably, said first bias voltage is higher by a given level than a source voltage, said second bias voltage being a negative value, said third bias voltage being ground voltage, and said fourth bias voltage being said source voltage.

Alternatively, said first bias voltage may be lower by a given level than a source voltage, said second bias voltage being a negative value, said third bias voltage being ground voltage, and said fourth bias voltage being said source voltage.

According to a second aspect of the invention, there is provided a semiconductor device with a memory cell array region and a peripheral circuit region integrated in a first-conductivity-type substrate, comprising:

a first second-conductivity-type well with a first-conductivity-type MOS transistor formed in said memory cell array region and applied with a first bias voltage;

a first first-conductivity-type well with a second-conductivity-type MOS transistor formed in said first second-conductivity-type well and applied with a second bias voltage;

a second first-conductivity-type well with a second-conductivity-type MOS transistor formed in said peripheral circuit region and applied with a third bias voltage; and

a second second-conductivity-type well with a first-conductivity-type MOS transistor formed in said peripheral circuit region separately from said second first-conductivity-type well and applied with said first bias voltage.

Preferably, said first-conductivity-type substrate comprises a highly concentrated first-conductivity-type diffusion region connected with said third bias voltage.

Preferably, said first bias voltage is a source voltage, said second bias voltage being a negative voltage, and said third bias voltage being ground voltage.

Preferably, a negative voltage generator is provided for generating said negative voltage.

According to a third aspect of the invention, there is provided a semiconductor device with a memory cell array region and peripheral circuit region integrated in a first-conductivity-type substrate, comprising:

a first second-conductivity-type well with a first-conductivity-type MOS transistor formed in said memory cell array region and applied with a first bias voltage;

a first first-conductivity-type well with a second-conductivity-type MOS transistor formed in said first second-conductivity-type well and applied with a second bias voltage;

a second first-conductivity-type well with a second-conductivity-type MOS transistor formed in said peripheral circuit region and applied with said second bias voltage; and

a second second-conductivity-type well with a first-conductivity-type MOS transistor formed in said peripheral circuit region separately from said second first-conductivity-type well and applied with a third bias voltage.

Preferably, said first-conductivity-type substrate comprises a highly concentrated first-conductivity-type diffusion region isolated from said wells and connected with said second bias voltage.

Said first bias voltage may be higher by a given level than a source voltage, said second bias voltage may be ground voltage, and said third bias voltage may be said source voltage.

Alternatively, said first bias voltage may be higher by a given level than a source voltage, said second bias voltage may be a negative voltage, and said third bias voltage may be said source voltage.

Said first-conductivity-type substrate comprises a highly concentrated first-conductivity-type diffusion region connected with said ground voltage.

Preferably, a voltage pumping circuit is provided for generating a voltage higher by a given level than said source voltage.

Said first bias voltage may be lower by a given level than a source voltage, said second bias voltage may be a negative voltage, and said third bias voltage may be said source voltage.

Said first bias voltage may be lower by a given level than said source voltage, said second bias voltage may be negative voltage, and said third bias voltage may be lower by a given level than said source voltage.

An internal voltage generator may be provided for generating a voltage lower by a given level than said source voltage.

According to a fourth aspect of the invention, there is provided a semiconductor device with a memory cell array region and peripheral circuit region integrated in a first-conductivity-type substrate, said memory cell array region having a plurality of word lines, bit lines, memory cells, sense amplifiers, row decoders and word line drivers, said peripheral circuit region having a plurality of TTL input buffers and data output drivers, comprising:

a first group of power supply pads for only supplying said memory cell array region;

a second group of power supply pads for only supplying said peripheral circuit region;

a third group of power supply pads for only supplying said plurality of word lines and TTL input buffers;

a fourth group of power supply pads for only supplying said data output drivers;

first second-conductivity-type wells with at least first first-conductivity-type wells formed in said memory cell array region and connected with said first group of power supply pads;

second second-conductivity-type wells having at least second first-conductivity-type wells formed in said peripheral circuit region and connected with said second group of power supply pads;

a first plurality of second-conductivity-type MOS transistors formed in said first first-conductivity-type wells and connected with said third group of power supply pads; and

a second plurality of second-conductivity-type MOS transistors formed in said second first-conductivity-type wells and connected with said fourth group of power supply pads.

According to a fifth aspect of the invention there is provided a semiconductor device comprising:

a first-conductivity-type substrate;

a second-conductivity-type well formed in said substrate;

a first second-conductivity-type MOS transistor and first highly concentrated first-conductivity-type diffusion region formed in said first-conductivity-type well:

a second first-conductivity-type MOS transistor and second highly concentrated second-conductivity-type diffusion region; and

a third highly concentrated first-conductivity-type diffusion region formed in said first-conductivity-type substrate:

wherein the source and drain of said first MOS transistor, said first highly concentrated diffusion region, the gate of said second MOS transistor, and said third highly concentrated diffusion region are commonly connected,

wherein the gate of said first MOS transistor, the drain and source of said second MOS transistor, and said second highly concentrated diffusion region are commonly connected.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to Figures 3 to 11 of the accompanying diagrammatic drawings, in which:

Figure 3A, 3B and 3C illustrate one example of an embodiment of the present invention;

Figures 4A and 4B illustrate another embodiment of the present invention respectively applied to a memory cell array region and peripheral circuit region;

Figure 5 illustrates power supply pads which may be applied to the embodiments of Figures 3A, 3B and 3C and Figures 4A and 4B;

Figure 6 is a preferred embodiment of the present invention according to Figures 3A, 3B and 3C and Figures 4A and 4B and Figure 5;

Figure 7 illustrates the construction of MOS capacitors;

Figure 8 illustrates processing steps for forming a triple-well which may be employed in an embodiment of the present invention; and

Figures 9, 10 and 11 respectively illustrate the output characteristics of a negative voltage generator, voltage pump circuit and internal voltage generator.

Figure 3 shows how a well bias voltage (or a backgate voltage) may be applied to a device as shown in Figure 2. Referring to Figure 3A, the well bias voltage applied to a P-well 23 of a memory array region 100 is a negative voltage V_{BB}. Further, a ground voltage Vss is applied to a P-well 24 of a peripheral circuit region 400 . The well bias voltage applied to N-wells 22 and 25 formed in the memory array and peripheral circuit regions is a source voltage Vcc. The P-well 23 of the memory array region has the negative voltage applied to it so as to reverse bias the junction between the P-well and an N+ diffusion region that is a drain of the NMOS transistor 31, thus reducing the bit line capacitance. This reduces the ratio C_B/Cs of bit line capacitance C_B to memory cell storage capacitance Cs. In addition, the well bias voltages applied to the P-wells of the memory cell array and peripheral circuit regions are respectively negative and ground voltages so as to prevent or reduce interference noise. Further, the peripheral circuit region supplies the ground voltage to the P-well 24, so that the latch-up phenomenon due to the short channel is considerably reduced compared to the prior art.

Referring to Figure 3B, in a peripheral circuit region 400 the source voltage Vcc is applied to an N-well 25 and the ground voltage Vss or

backgate voltage V_{BB} is applied to P-well 24, while in a memory cell array region 100 an N-well 22 is applied with a higher voltage Vpp, hereinafter referred to as "pumping voltage", than the source voltage and a P-well 23 has a ground or negative voltage applied to it. The pumping voltage Vpp is generated by a high voltage generator arranged in a semiconductor memory device. In this case, it is necessary that the noise caused by the source voltage of the peripheral circuit region should not adversely affect the memory cell array region.

Referring to Figure 3C, in a peripheral circuit region 400 an N-well 25 is supplied with a source voltage Vcc or a voltage V_{INT}, hereinafter referred to as "internal voltage", which is lower than the source voltage Vcc and a P-well 24 is supplied with a ground voltage or negative voltage, while in a memory cell array region 100 an N-well 22 is supplied with the internal voltage V_{INT} and a P-well 23 with the ground voltage Vss or negative voltage V_{BB}. This produces the same effect as Figure 3B.

Referring to Figure 4A, in a P-type substrate 70 there are formed two isolated N-wells 71 and 72. The N-well 71 has a P-well 73 with an NMOS transistor 74 constituting an N-type sense amplifier in a memory cell array region. Similarly, a PMOS transistor 75 formed in the N-well 72 constitutes a P-type sense amplifier in the memory cell array region. The P-well 73 is supplied with a negative voltage V_{BB} as a well bias voltage (or a backgate voltage), the N-well 71 enclosing the P-well 73 is supplied with a pumping voltage Vpp or internal voltage V_{INT}, and the N-well 72 isolated from the N-well 71 is supplied with a source voltage Vcc. Thus the noise induced by the source voltage does not interfere with the well bias voltage of the P-well 73, thus stabilizing the function of the semiconductor memory device.

Referring to Figure 4B which shows a peripheral circuit region, an N-well 81 encloses a P-well 83 with an NMOS transistor 86, while an N-well 82 encloses a P-well 84 with NMOS transistors 87 and 88 separated from the N-well 81. It is noted that the transistor 86 is an NMOS transistor of a TTL input buffer and the transistors 87 and 88 form a data output buffer/output driver (see Figure 1E). Backgate voltages (or bias voltages of P-wells) of the NMOS transistors are all the negative voltage V_{BB}. The P-wells 83 and 84 are separated from the substrate 70 via the respective N-wells 81 and 82, which are supplied with the source voltage Vcc from separated power supply pads.

Conventionally, since the power supply pads for a semiconductor memory device consist of a single source voltage pad and a single ground voltage pad, the noise induced in the voltage source used in the peripheral circuit region affects a memory array region. In order to resolve this problem, embodiments of the present invention may employ, as shown in Figure 5, a plurality of power supply pads V_{CCLA}, V_{CCRA}, V_{SSLA}, V_{SSRA} for a memory array and power supply pads V_{CCLP}, V_{CCRP}, V_{SSLP}, V_{SSLP} for a peripheral circuit. In this case, the power supply pads V_{CCLA}, V_{CCLP}, V_{SSLA}, V_{SSLP} are used for the left side and the power supply pads V_{CCRA}, V_{CCRP}, V_{SSRA}, V_{SSRP} for the right side. Further left and right ground voltage pads V_{SSLQ} and V_{SSRQ} are provided for a word line/TTL input buffer. An additional voltage source pad V_{CCRD} and ground voltage pad V_{SSRD} are provided for a data output driver. Thus the noise induced in one pad is not transferred to another.

An example of the operation of a circuit embodying the invention will now be described with reference to Figure 6. In a P-type semiconductor substrate 70 a memory cell array region 100 has separated first and second N-

wells 22 and 91, and a peripheral circuit region 400 has separated third, fourth and fifth N-wells 25, 81 and 82 and a first P-well 24. The first N-well 22 is provided with a second P-well 23 and first PMOS transistor 32. The second P-well 23 is provided with a first NMOS transistor 31 used in a memory cell, N-type sense amplifier, input/output gate, row decoder/word line driver and equalization circuit. A backgate voltage of the first NMOS transistor 31 (or a bias voltage of the second P-well 23) is a negative voltage V_{BB}. The first PMOS transistor 32 is used for a P-channel sense amplifier and its backgate voltage is a array source voltage V_{CCA} (V_{CCLA} or V_{CCRA}). A second PMOS transistor 92 formed in the second N-well 91 is used for a word line drive clock pulse generator (Figure 1C) and its backgate voltage (or a well bias voltage of the second N-well) is a pumping voltage Vpp. The third N-well 25 of the peripheral circuit region 400 is provided with a PMOS transistor 34 whose backgate voltage is a peripheral voltage source V_{CCP} (V_{CCLP} or V_{CCRP}). In the first P-well 24 is formed an NMOS transistor 33 whose backgate voltage (or a bias voltage of the first P-well) is a peripheral ground voltage V_{SSP} (V_{SSLP} or V_{SSRP}). In the fourth N-well 81 is formed a third P-well 83 with an NMOS transistor 86 whose backgate voltage is the negative voltage V_{BB}. A ground voltage applied to a source of the transistor 86 is a ground voltage V_{SSQ} (V_{SSLQ} or V_{SSRQ}) for a word line and TTL input buffer. In the fifth N-well 82 is formed a fourth P-well 84 with NMOS transistors 87 and 88 for the output of Figure 1E. A source of the transistor 88 is supplied with a driver ground voltage V_{SSD}, and a drain of the transistor 87 with a driver source voltage V_{CCD}. A backgate voltage of the transistors 87 and 88 (or the bias voltage of the fourth P-well) is the negative voltage V_{BB}. The fifth N-well 82 is supplied with a peripheral source voltage V_{CCP} (V_{CCLP} or V_{CCRP}).

It will readily appreciated by one skilled in the art that the bias voltages (or the backgate voltages of the transistors) applied to the wells may be differently set. Of course, the embodiment of Figure 6 may also be applied to an N-type substrate.

Referring to Figure 7, the inventive triple-well structure may be employed to construct a MOS capacitor. As shown in Figure 7A, a first common electrode applied with the source voltage Vcc is obtained by connecting a gate 111 of an NMOS transistor, P+ diffusion regions 107 and 108 and an N+ diffusion region 109 formed in an N-well 102. Further, a second common electrode applied with a ground voltage Vss is obtained by connecting N+ diffusion regions 104 and 105 formed in a P-well 103, a P+ diffusion region 106 for supplying a backgate voltage, a P+ diffusion region 110 formed in a substrate 101 and a gate 112 of a PMOS transistor. There is then produced a capacitor structure consisting of parallel connected NMOS and PMOS capacitors. Referring to Figure 7B, PMOS and NMOS capacitors are connected in series and a source of clock pulses applied to their gates. In this case, all the diffusion regions formed in a P-well are commonly connected to ground, and all the diffusion regions formed in an N-well connected to a source voltage. Besides these specific embodiments further variations may be envisaged.

Figure 8 illustrates the processing steps for fabricating a triple-well structure. It is readily appreciated that a P-type silicon single crystal substrate 1 is used for the substrate. The substrate 1 is sequentially covered with an oxide layer 2 and nitride layer 3 as shown in Figure 8A. A photoresist pattern 4 is formed on the nitride layer 3 to selectively etch the nitride and oxide layers 3 and 2 so as to form window 5, through which window are

implanted impurity ions of the fifth element group such as arsenic and phosphorous to form an N-well, as shown in Figure 8B. Referring to Figure 8C, an exposed surface of the substrate is subjected to wet oxidation and the implanted impurity ions are diffused to form an N-well 7. The exposed surface of the substrate is covered with a thick oxide layer 6. In the step of Figure 8D, after removing the thick oxide layer 6, and the remaining oxide and nitride layers 2 and 3, a thin pad oxide layer 8 is deposited on to the substrate. A second photoresist pattern 9 is formed on the thin pad oxide layer 8 and impurity ions of the third element group such as boron are implanted. Then, as shown in Figure 8E, there are formed P-wells 10 and 11 inside and outside the N-well 7. Thereafter there are formed transistors required for the wells and corresponding contact diffusion regions for a backgate voltage (or well bias voltage).

Figures 9, 10 and 11 respectively show the output characteristics of the negative voltage (V_{BB}) generator, pumping voltage (Vpp) generator and internal voltage (V_{INT}) generator of the present invention. The negative voltage generator and internal voltage generator are generally used in DRAMs. The characteristics of the pumping voltage generator is well disclosed in IEEE JSSC, Aug. 1991, pp1171.

Although the above embodiments are used for the P-type substrate, they may also be used for an N-type substrate. In addition, embodiments of the present invention may be employed in any devices fabricated by the CMOS process together with DRAMs.

The term "ground potential" (or like terms such as "ground voltage" or "earth" potential or voltage) is used conveniently in this specification to

denote a reference potential. As will be understood by those skilled in the art, although such reference potential may typically be zero potential, it is not essential that it is so, and may be a reference potential other than zero.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS:

1. A semiconductor device comprising:

a first second-conductivity-type well formed on a first-conductivity-type semiconductor substrate and arranged to receive a first bias voltage;

a first-conductivity-type well formed in said first second-conductivity-type well and arranged to receive a second bias voltage; and

a second second-conductivity-type well formed in said first-conductivity-type well and connected to said second bias voltage.

2. A semiconductor device as claimed in Claim 1, wherein said first-conductivity-type semiconductor substrate is arranged to receive a third bias voltage.

3. A semiconductor device as claimed in Claim 1 or 2, wherein said first-conductivity-type well comprises an active region of a second-conductivity-type MOS transistor.

4. A semiconductor device as claimed in Claim 1, 2 or 3, wherein at least one of said second-conductivity-type wells comprises a first-conductivity-type MOS transistor.

5. A semiconductor device as claimed in any of the preceding claims, further comprising another second-conductivity-type well with a first-conductivity-type MOS transistor isolated from said second-conductivity-type well and arranged to receive a fourth bias voltage.

6. A semiconductor device as claimed in Claim 5, wherein said first bias voltage is higher by a given level than a source voltage, said second bias voltage being a negative value, said third bias voltage being ground voltage, and said fourth bias voltage being said source voltage.

7. A semiconductor device as claimed in Claim 5, wherein said first bias voltage is lower by a given level than a source voltage, said second bias voltage being a negative value, said third bias voltage being ground voltage, and said fourth bias voltage being said source voltage.

8. A semiconductor device with a memory cell array region and a peripheral circuit region integrated in a first-conductivity-type substrate, comprising:

a first second-conductivity-type well with a first-conductivity-type MOS transistor formed in said memory cell array region and applied with a first bias voltage;

a first first-conductivity-type well with a second-conductivity-type MOS transistor formed in said first second-conductivity-type well and applied with a second bias voltage;

a second first-conductivity-type well with a second-conductivity-type MOS transistor formed in said peripheral circuit region and applied with a third bias voltage; and

a second second-conductivity-type well with a first-conductivity-type MOS transistor formed in said peripheral circuit region separately from said second first-conductivity-type well and applied with said first bias voltage.

9. A semiconductor device as claimed in Claim 8, wherein said first-conductivity-type substrate comprises a highly concentrated first-conductivity-type diffusion region connected with said third bias voltage.

10. A semiconductor device as claimed in Claim 8 or 9, wherein said first bias voltage is a source voltage, said second bias voltage being a negative voltage, and said third bias voltage being ground voltage.

11. A semiconductor device as claimed in Claim 10, further comprising a negative voltage generator for generating said negative voltage.

12. A semiconductor device with a memory cell array region and peripheral circuit region integrated in a first-conductivity-type substrate, comprising:

a first second-conductivity-type well with a first-conductivity-type MOS transistor formed in said memory cell array region and applied with a first bias voltage;

a first first-conductivity-type well with a second-conductivity-type MOS transistor formed in said first second-conductivity-type well and applied with a second bias voltage;

a second first-conductivity-type well with a second-conductivity-type MOS transistor formed in said peripheral circuit region and applied with said second bias voltage; and

a second second-conductivity-type well with a first-conductivity-type MOS transistor formed in said peripheral circuit region separately from said second first-conductivity-type well and applied with a third bias voltage.

13. A semiconductor device as claimed in Claim 12, wherein said first-conductivity-type substrate comprises a highly concentrated first-conductivity-type diffusion region isolated from said wells and connected with said second bias voltage.

14. A semiconductor device as claimed in Claim 12 or 13, wherein said first bias voltage is higher by a given level than a source voltage, said second bias voltage being ground voltage, and said third bias voltage being said source voltage.

15. A semiconductor device as claimed in Claim 12, wherein said first bias voltage is higher by a given level than a source voltage, said second bias voltage being a negative voltage, and said third bias voltage being said source voltage.

16. A semiconductor device as claimed in Claim 15, wherein said first-conductivity-type substrate comprises a highly concentrated first-conductivity-type diffusion region connected with said ground voltage.

17. A semiconductor device as claimed in Claim 14, 15 or 16, further comprising a voltage pumping circuit for generating a voltage higher by a given level than said source voltage.

18. A semiconductor device as claimed in Claim 12 or 13 wherein said first bias voltage is lower by a given level than a source voltage, said second bias voltage being a negative voltage, and said third bias voltage being said source voltage.

19. A semiconductor device as claimed in Claim 12 or 13, wherein said first bias voltage is lower by a given level than said source voltage, said second bias voltage being a negative voltage, and said third bias voltage being lower by a given level than said source voltage.

20. A semiconductor device as claimed in any one of claims 14 to 19, further comprising an internal voltage generator for generating a voltage lower by a given level than said source voltage.

21. A semiconductor device with a memory cell array region and peripheral circuit region integrated in a first-conductivity-type substrate, said memory cell array region having a plurality of word lines, bit lines, memory cells, sense amplifiers, row decoders and word line drivers, said peripheral circuit region having a plurality of TTL input buffers and data output drivers, comprising:

a first group of power supply pads for only supplying said memory cell array region;

a second group of power supply pads for only supplying said peripheral circuit region;

a third group of power supply pads for only supplying said plurality of word lines and TTL input buffers;

a fourth group of power supply pads for only supplying said data output drivers;

first second-conductivity-type wells with at least first first-conductivity-type wells formed in said memory cell array region and connected with said first group of power supply pads;

second second-conductivity-type wells having at least second first-conductivity-type wells formed in said peripheral circuit region and connected with said second group of power supply pads;

a first plurality of second-conductivity-type MOS transistors formed in said first first-conductivity-type wells and connected with said third group of power supply pads; and

a second plurality of second-conductivity-type MOS transistors formed in said second first-conductivity-type wells and connected with said fourth group of power supply pads.

22. A semiconductor device comprising:

a first-conductivity-type substrate;

a second-conductivity-type well formed in said substrate;

a first second-conductivity-type MOS transistor and first highly concentrated first-conductivity-type diffusion region formed in said first-conductivity-type well:

a second first-conductivity-type MOS transistor and second highly concentrated second-conductivity-type diffusion region; and

a third highly concentrated first-conductivity-type diffusion region formed in said first-conductivity-type substrate:

wherein the source and drain of said first MOS transistor, said first highly concentrated diffusion region, the gate of said second MOS transistor, and said third highly concentrated diffusion region are commonly connected;

wherein the gate of said first MOS transistor, the drain and source of said second MOS transistor, and said second highly concentrated diffusion region are commonly connected.

23. A semiconductor device substantially as hereinbefore described with reference to Figures 3A to 3C or Figures 4A and 4B of the accompanying drawings.

24. A semiconductor device as claimed in claim 23 comprising power supply pads substantially as hereinbefore described with reference to Figure 5 of the accompanying drawings.

25. A semiconductor device substantially as hereinbefore described with reference to Figure 6 of the accompanying drawings.

26. A semiconductor device substantially as hereinbefore described with reference to Figures 6 to 11 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under section 17 (The Search Report)

Application number
GB 9304655.5

Relevant Technical fields

(i) UK Cl (Edition L) H1K (KGAF, KGAM)

(ii) Int Cl (Edition 5) H01L

Search Examiner
W A MORRIS

Databases (see over)
(i) UK Patent Office

(ii)

Date of Search
26 MAY 1993

Documents considered relevant following a search in respect of claims 1 TO 20

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	WO 90/08401 A1 (FRAUNHOFER) see Figure 1	1-5
X	US 5157281 (TEXAS) see Figure 2	1-5
X	Japio abstract of JP62-155555 and JP62-155555 (SONY) see abstract	1

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

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